AMENDMENTS TO THE CLAIMS

This listing of claim will replace all prior versions and listings of claim in the application.

1. (currently amended) A memory system including a control path to a host device, the host device supplying a host voltage having a level suitable for operation of the memory system and a power up complete signal indicating that the host voltage has reached the level, comprising:

a voltage regulator including a host voltage input, an output and a bypass shorting the host voltage at the input to the output;

a controller;

a voltage detector communicating with the regulator and the controller;

a bypass enable signal output by the controller subsequent to the power up complete signal being generated by the host device indicating that the host voltage has reached the level~~power up of the host is complete~~.

2. (currently amended) The memory system of claim 1 wherein the power up complete signal generated by the host device ~~indicates that the power up of the host is complete and~~ is provided via the control path.

3. (original) The memory system of claim 1 wherein the bypass is at least one transistor.

4. (original) The memory system of claim 3 wherein the bypass comprises a plurality of transistors.

5. (original) The memory system of claim 3 wherein the bypass enable signal is provided by the controller to a gate of the transistor.

6. (original) The memory system of claim 1 wherein the signal generated by the host device is a command signal to the memory system.

7. (original) The memory system of claim 1 wherein the memory system is a multimedia card.

8. (original) The memory system of claim 1 wherein the memory system is a multimedia card and the signal generated by the host device is a command signal.

9. (original) The memory system of claim 8 wherein the command signal is CMD0 or CMD1.

10. (previously presented) The memory system of claim 2 wherein the voltage detector outputs a bypass enable signal shorting the input voltage to the output when the host supply voltage is below a threshold. .

11. (original) The memory system of claim 1 wherein the memory system is a pc card.

12. (original) The memory system of claim 1 wherein the memory system is a compact flash card.

13. (original) The memory system of claim 1 wherein the memory system is a secure digital card.

14. (original) The memory system of claim 1 wherein the memory system is a smart media card.

15. (original) The memory system of claim 1 wherein the memory system is a memory

stick.

16. (currently amended) A method for operating a voltage regulator in a memory system including a controller, comprising:

providing a voltage regulator having a host voltage input and an output, and including a regulator bypass responsive to the controller shorting the host voltage at the input to the output responsive to an enable signal;

setting the bypass to off prior to power up of a host device;

responsive to a power up completion signal from a host device to the controller, the power up completion signal indicating that the host voltage is at a level suitable for operation of the memory system, determining the power supplied by the host; and

if the power is below a threshold operating voltage, enabling the bypass using the controller.

17. (original) The method of claim 16 wherein the bypass is a transistor and the step of setting the bypass to off includes providing a signal to a gate of the transistor.

18. (original) The method of claim 17 wherein the bypass comprises a plurality of transistors and the step of enabling the bypass comprises applying an enable signal to each gate of said plurality of transistors.

19. (original) The method of claim 17 wherein the power up completion signal is a command signal from the host.

20. (original) The method of claim 19 wherein command signal is CMD0 or CMD1 for a multimedia card.

21. (original) The method of claim 17 wherein the threshold voltage is below 2.7 volts.

22. (original) The method of claim 17 wherein the threshold voltage is below 2.0 volts.

23. (original) The method of claim 17 wherein the threshold voltage is below 1.65 volts.

24. (original) The method of claim 17 wherein the threshold voltage is below 1.3 volts.

25. (currently amended) A peripheral device for a host system supplying a host voltage, the peripheral device including a voltage regulator circuit and a controller, comprising:

a voltage regulator having a host voltage input and an output;

a bypass element coupled to selectively short the host voltage at the input to the output;

a bypass control signal output from the controller coupled to the bypass element and responsive to a host system power up completed signal indicating that the host voltage is at a level suitable for operation of the memory system and which enables the bypass element when the host voltage is below a threshold level subsequent to host power-up completion.

26. (original) The peripheral device of claim 25 wherein the regulator includes a detector responsive to the power up completed signal.

27. (previously presented) The peripheral device of claim 26 wherein the detector outputs a first signal when the voltage provided by the host is above the threshold level and a second signal when the host is below the threshold level.

28. (original) The peripheral device of claim 25 wherein the bypass element includes at least one p-type transistor.

29. (original) The peripheral device of claim 27 wherein the bypass control signal is applied to the gate of the at least one transistor.

30. (original) The peripheral device of claim 27 wherein the bypass element is disabled during power up of the host device.

31. (original) The peripheral device of claim 25 wherein the bypass control signal is provided by a controller.

32. (currently amended) A method for operating a voltage regulator in a multimedia card memory device, comprising:

providing a voltage regulator having a host voltage input and an output, a controller, and including a regulator bypass shorting a host voltage at the input to the output;

setting the bypass to off prior to power up of a host device;

responsive to a command signal from the host device indicating that the host voltage is at a level suitable for operation of the memory system, determining the power supplied by the host; and

if the power is below a threshold operating voltage subsequent to ~~host power-up completion~~the command signal, enabling the bypass using the controller.

33. (currently amended) The method of claim 32 wherein command signal is CMD0 or CMD1 ~~in~~ for a multimedia card.

34. (currently amended) A memory system, comprising:

a controller;

a memory array; and

a voltage regulator having a shorting element between a host voltage input and an output, the shorting element being responsive to a bypass control signal, the bypass control signal provided by the controller responsive to a host system power up complete signal indicating that the host voltage is at a level suitable for operation of the memory system which enables the shorting element when the host supply voltage provided by the host is below a threshold level subsequent to power-up

completion.

35. (original) The memory system of claim 34 wherein the regulator outputs a voltage less than the host supply voltage when said supply voltage is above said threshold.

36. (original) The memory system of claim 35 wherein the regulator outputs at least a first or a second output voltage when said host supply voltage is above said threshold.